

WHAT IS CLAIMED:

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- 1 1. A method including:
- 2
- 3 in a queue, writing a first instruction to a first location indicated by a
- 4 write pointer;
- 5
- 6 making a qualitative determination whether or not to retain the first
- 7 instruction within the queue;
- 8
- 9 if the qualitative determination is to retain the first instructions, then
- 10 advancing the write pointer to indicate a second location within the
- 11 queue into which to write a second instruction; and
- 12
- 13 if the qualitative determination is not to retain the first instruction,
- 14 then maintaining the write pointer to indicate the first location within
- 15 the queue into which to write the second instruction, so that the first
- 16 instruction is overwritten by the second instruction.
- 1 2. The method of claim 1 wherein the qualitative determination includes
- 2 examining a valid bit associated with the first instruction to determine
- 3 validity of the first instruction, making the qualitative determination to
- 4 retain the first instruction if the valid bit indicates the first instruction is

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5 being valid, and making the qualitative determination not to retain the first
6 instruction if the valid bit indicates the first instruction as being invalid.

1 3. The method of claim 2 wherein a plurality of instructions are written
2 to the queue as a set of a predetermined number of instructions, and
3 wherein at least one instruction of the set is indicated as being invalid by an
4 associated valid bit on the account of being outside a trace of instructions.

1 4. The method of claim 2 wherein a plurality of instructions are written
2 to the queue in a set of a predetermined number of instructions, and wherein
3 at least one instruction of the set is indicated as being invalid on account of a
4 branch misprediction relating to a branch instruction upstream of the at least
5 one instruction in a stream of instructions.

1 5. The method of claim 1 wherein the first instruction comprises a first
2 microinstruction.

1 6. The method of claim 5 wherein the first microinstruction is written to
2 the queue from a microinstruction cache.

1 7. The method of claim 6 wherein the first microinstruction is part of a
2 trace of microinstructions received from the microinstruction cache.

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1 8. The method of claim 6 wherein the first instruction is received from
2 an instruction source operating in a first clocking domain into the queue and
3 read from the queue to an instruction destination operating in a second
4 clocking domain.

1 9. The method of claim 1 wherein the first instruction is received into
2 the queue as part of a set of instructions comprising a first predetermined
3 number of instructions and read from the queue to an instruction
4 destination as part of a second set of instructions comprising a second
5 number of instructions.

1 10. The method of claim 1 wherein the first instruction is written from a
2 source to a destination, and wherein the queue comprises a first path
3 between source and destination, the method including propagating the first
4 instruction from the source to the destination via a second path, not
5 including the queue, if the queue is empty.

1 11. The method of claim 10 including selecting between the first and
2 second paths to receive the first instruction for propagation to the
3 destination.

1 12. The method of claim 1 wherein the queue includes a first portion to
2 support a first thread within a multithreaded environment and a second

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3 portion to support a second thread within the multithreaded environment,
4 and wherein the first location into which the first instruction is written is
5 located in the first portion if the first instruction comprises part of the first
6 thread.

1 13. Apparatus comprising:

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3 a queue for buffering a first instruction propagated from a source to a
4 destination; and

5

6 write logic to make a qualitative determination whether or not to
7 retain the first instruction within the queue; if the qualitative
8 determination is to retain the first instruction, to advance a write
9 pointer to indicate a second location within the queue into which to
10 write a second instruction; and, if the qualitative determination is not
11 to return the first instruction, to maintain the write pointer to indicate
12 the first location within the queue into which to write the second
13 instruction, so that the first instruction is overwritten by the second
14 instruction.

1 14. The apparatus of claim 13 wherein the write logic is to examine a
2 valid bit associated with the first instruction to determine validity of the first
3 instruction, to make the qualitative determination to retain the first

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4 instruction if the valid bit indicates the first instruction as being valid, and to
5 make the qualitative determination not to retain the first instruction if the
6 valid bit indicates the first bit as being invalid.

1 15. The apparatus of claim 14 wherein the first instruction is written to
2 the queue as part of a set including a predetermined number of instructions,
3 and wherein at least one instruction of the set is indicated as being invalid
4 by an associated invalid bit on account of being outside a trace of
5 instructions.

1 16. The apparatus of claim 14 wherein the first instruction is written to
2 the queue as part of a set of a predetermined number of instructions, and
3 wherein at least one instruction of the set is indicated as being invalid on
4 account of a branch misprediction relating to a branch instruction upstream
5 of the at least one instruction in a stream of instructions.

1 17. The apparatus of claim 1 wherein the first instruction is a first
2 microinstruction.

1 18. The apparatus of claim 17 wherein the source from which the first
2 microinstruction is written to the queue comprises a microinstruction cache.

1 19. The apparatus of claim 18 wherein the first microinstruction is part of

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2 a trace of microinstructions received from the microinstruction cache.

1 20. The apparatus of claim 13 wherein the queue comprises a first path
2 between the source and the destination, the apparatus including a second
3 path between the source and destination, not including the queue, and
4 wherein the write logic directs the first microinstruction to be propagated
5 between the source and destination via the second path if the queue is
6 empty.

1 21. A machine-readable medium storing a sequence of instructions that,
2 when executed by machine, cause the machine to perform the steps of:

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4 in a queue, writing a first instruction to a first location indicated by a
5 write pointer;

6
7 making a qualitative determination whether or not to retain the first
8 instruction within the queue;

9
10 if the qualitative determination is to retain the first instructions, then
11 advancing the write pointer to indicate a second location within the
12 queue into which to write a second instruction; and

13
14 if the qualitative determination is not to retain the first instruction,

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15 then maintaining the write pointer to indicate the first location within
16 the queue into which to write the second instruction, so that the first
17 instruction is overwritten by the second instruction.

1 22. The machine-readable medium of claim 21 wherein the sequence of
2 instructions cause a multiprocessor to perform the step of examining a valid
3 bit associated with the instruction to determine validity of the first
4 instruction, to make the qualitative determination to retain the first
5 instruction if the valid bit indicates the first instruction as being valid, and to
6 make the qualitative determination not to retain the first instruction if the
7 valid bit indicates the first instruction as being invalid.